Amendments to the Claims

Amend claim 1 as follows:

1. (Currently Amended) A transparent latch circuit comprising:

a first latch circuit for receiving a data signal and latching the data signal in response to ~~at least one of~~ a first signal fluctuating periodically ~~and a test signal in the active state~~;

a second latch circuit for receiving an output signal of said first latch circuit and latching the output signal of said first latch circuit in response to an unasserted latch stop signal ~~at least one of a second signal complementary to the first signal and~~ when a test signal is in the active state; and

latch stop means for producing the latch stop signal while ~~for~~ receiving ~~an externally input test~~ the test signal and ~~one of~~ said first signal ~~or second signals~~ and causing ~~one of said first and~~ said second latch circuit ~~circuits~~ to have the data signal received by the transparent latch circuit pass therethrough when the test signal is in an inactive state and the latch stop signal is asserted.

2. (Currently Amended) The transparent latch circuit of claim 1, wherein said latch stop means comprises:

a logic gate for receiving the first signal and the test signal, and outputting the ~~second~~ unasserted latch stop signal when the test signal is in the active state, or ~~for~~ outputting ~~a~~ an asserted latch stop signal when the test signal is in the inactive state; and said second latch circuit permits the signal output by the first latch circuit to pass through during a concurrent period ~~wherein~~ when said second latch circuit receives ~~a latch~~ the asserted latch stop signal.

3. (Cancelled)

4. (Cancelled)

5. (New) A transparent latch circuit comprising:

a slave latch circuit for receiving an output signal from a master latch circuit and latching the output signal in response to a first signal fluctuating periodically;

a master latch circuit for receiving a data signal and a latch stop signal and latching the data signal in response to the unasserted latch stop signal, wherein the latch stop signal is unasserted when a test signal input is in the active state; and

a latch stop means for producing the latch stop signal while receiving the test signal and said first signal and causing said master latch circuit to have the data signal received by the transparent latch circuit pass therethrough when the test signal is in the inactive state and the latch stop signal is asserted.

6. (New) The transparent latch circuit of claim 5, wherein said latch stop means comprises:

a logic gate for receiving the first signal and the test signal, and outputting the unasserted latch stop signal when the test signal is in the active state or outputting an asserted latch stop signal when the test signal is in the inactive state; and

said master latch circuit permits the data signal to pass through during a concurrent period when said master latch circuit receives the asserted latch stop signal.

7. (New) A transparent latch circuit comprising,

at least one first transparent latch circuit having a first latch stop means, a first latch circuit and a second latch circuit, wherein the first latch stop means is coupled to the second latch circuit;

and at least one second transparent latch circuit having a second latch stop means, a third latch circuit, and a fourth latch circuit, wherein the second latch stop means is coupled to the third latch circuit

wherein said first latch stop means causes the second latch circuit to pass an output signal from the first latch circuit therethrough when a test signal is in an active state and wherein said second latch

stop means causes the third latch circuit to pass an output signal from a data signal input therethrough when the test signal is in the active state; and

said first and second transparent latch circuits are alternately interconnected.